0051601 2T5E9960

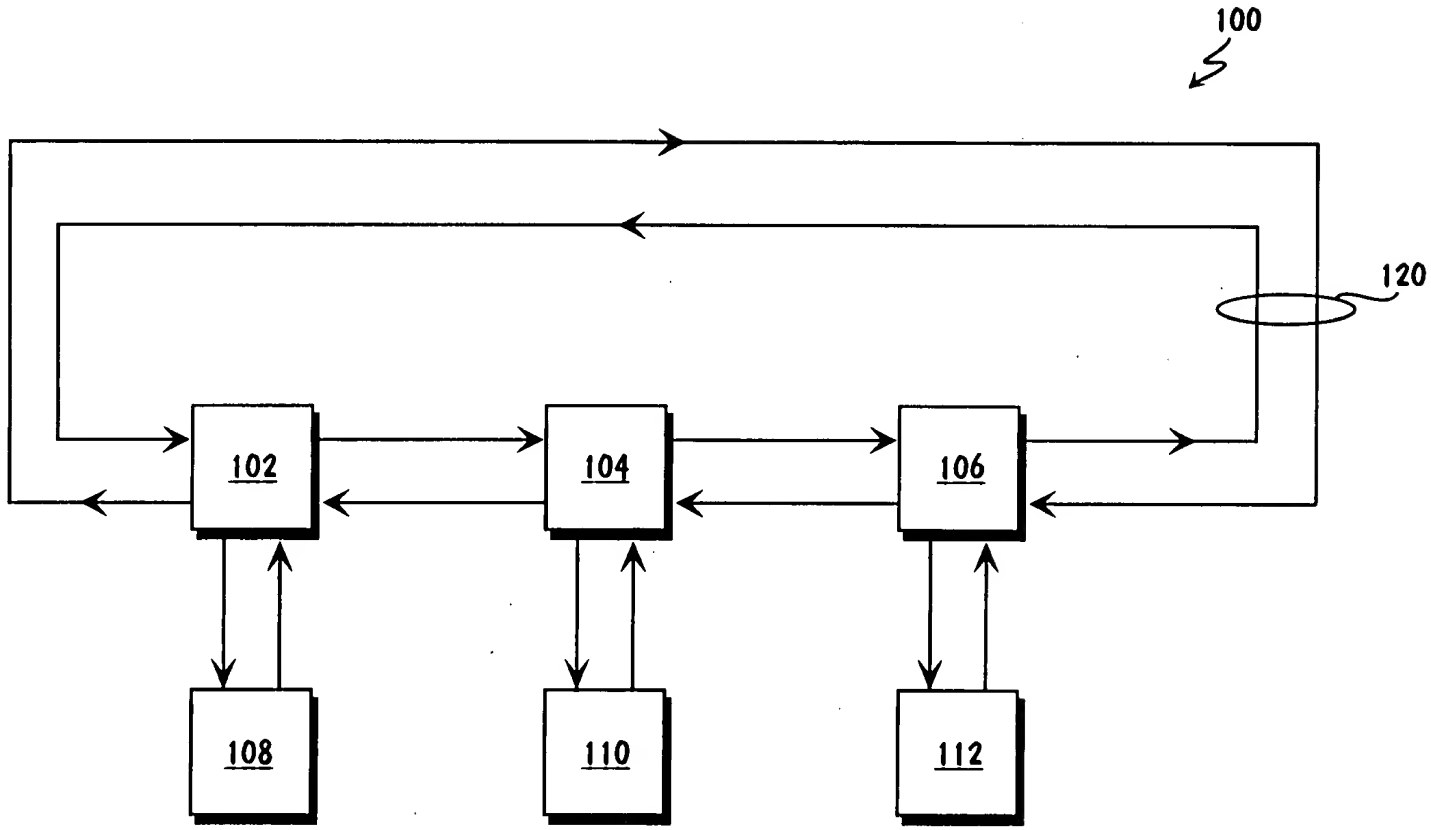


FIG. 1 (PRIOR ART)

00S160"2T5E9960

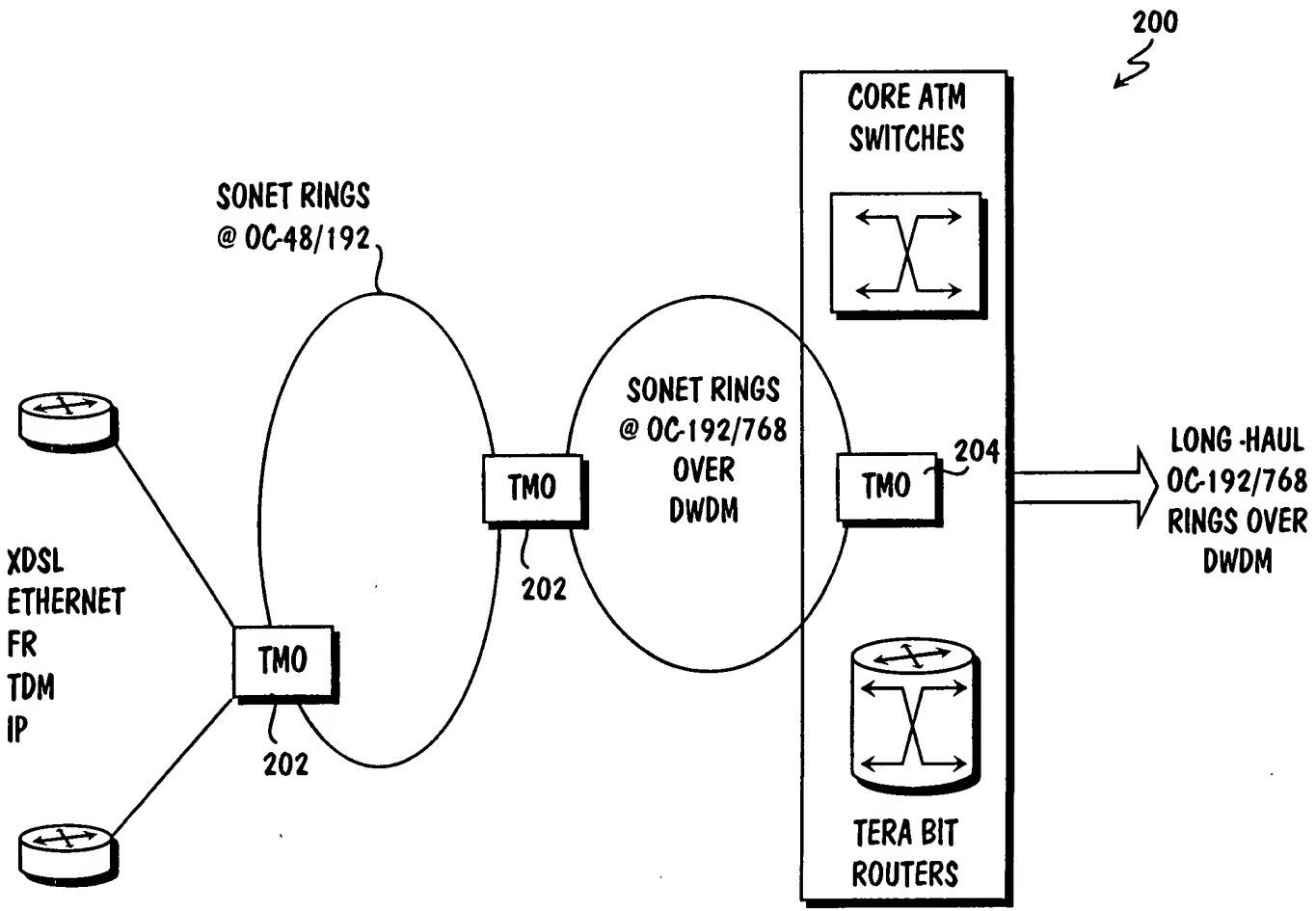


FIG. 2

0057602 2TSE960

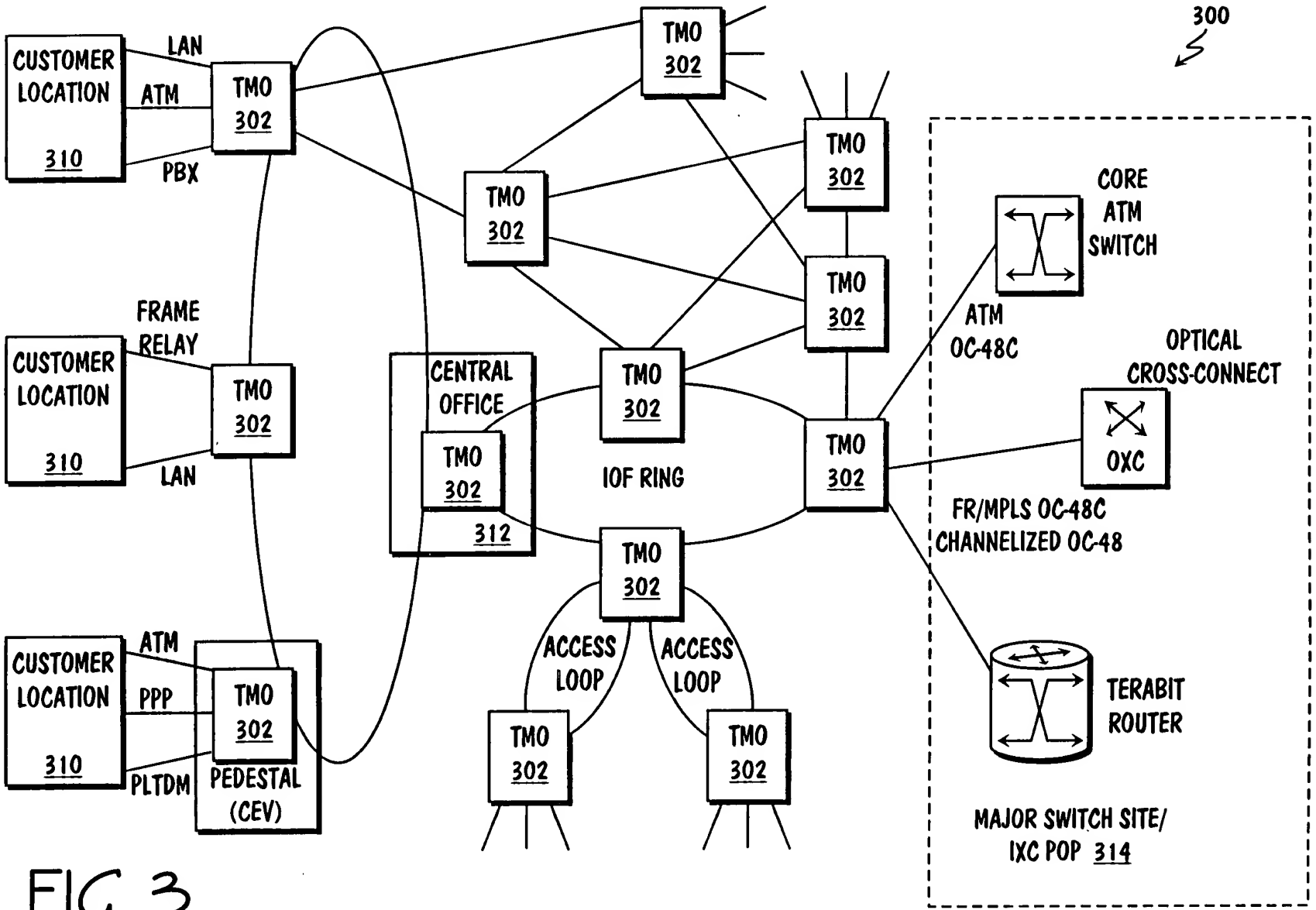


FIG. 3

005760 "2T5E9960

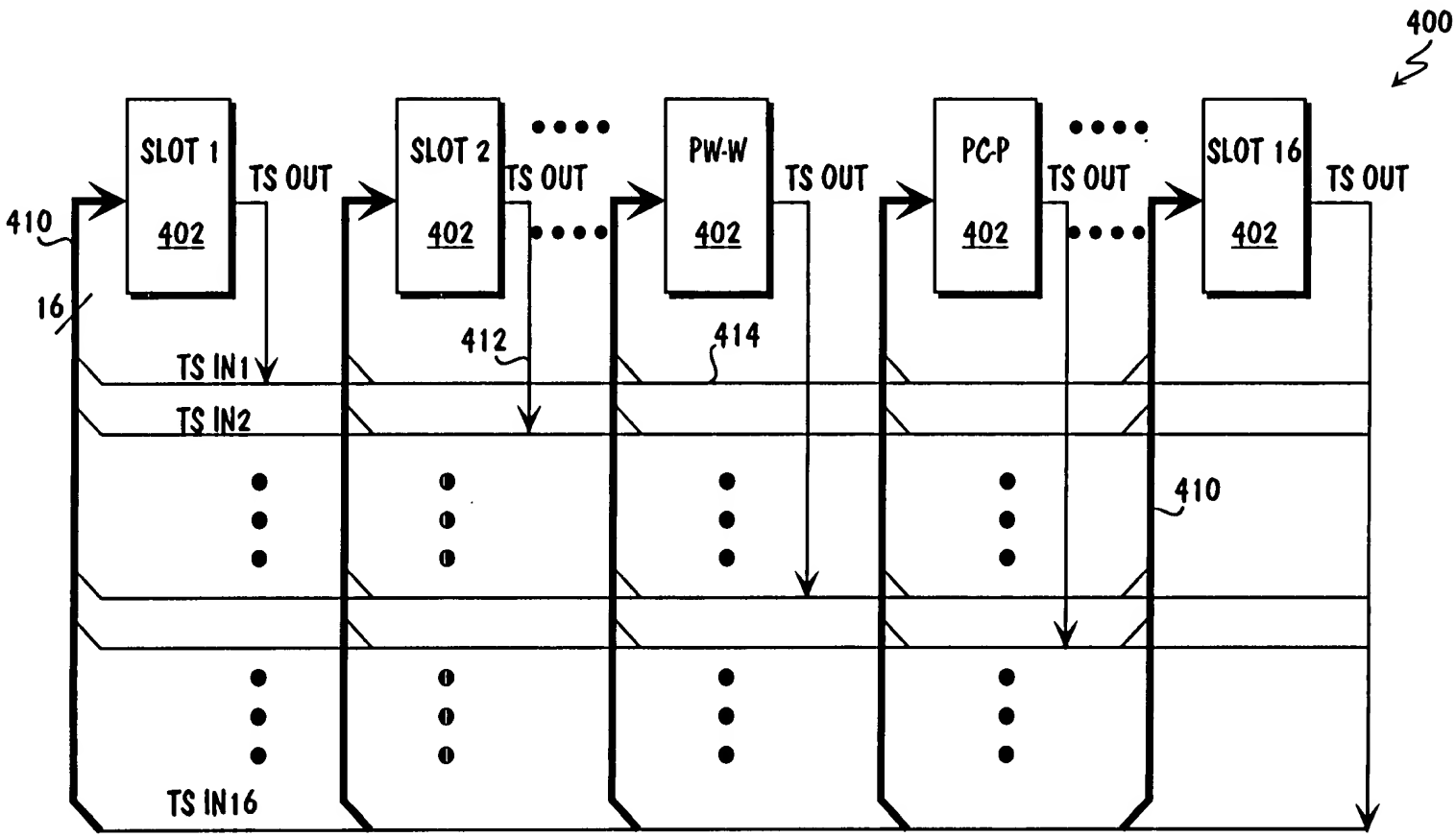


FIG. 4

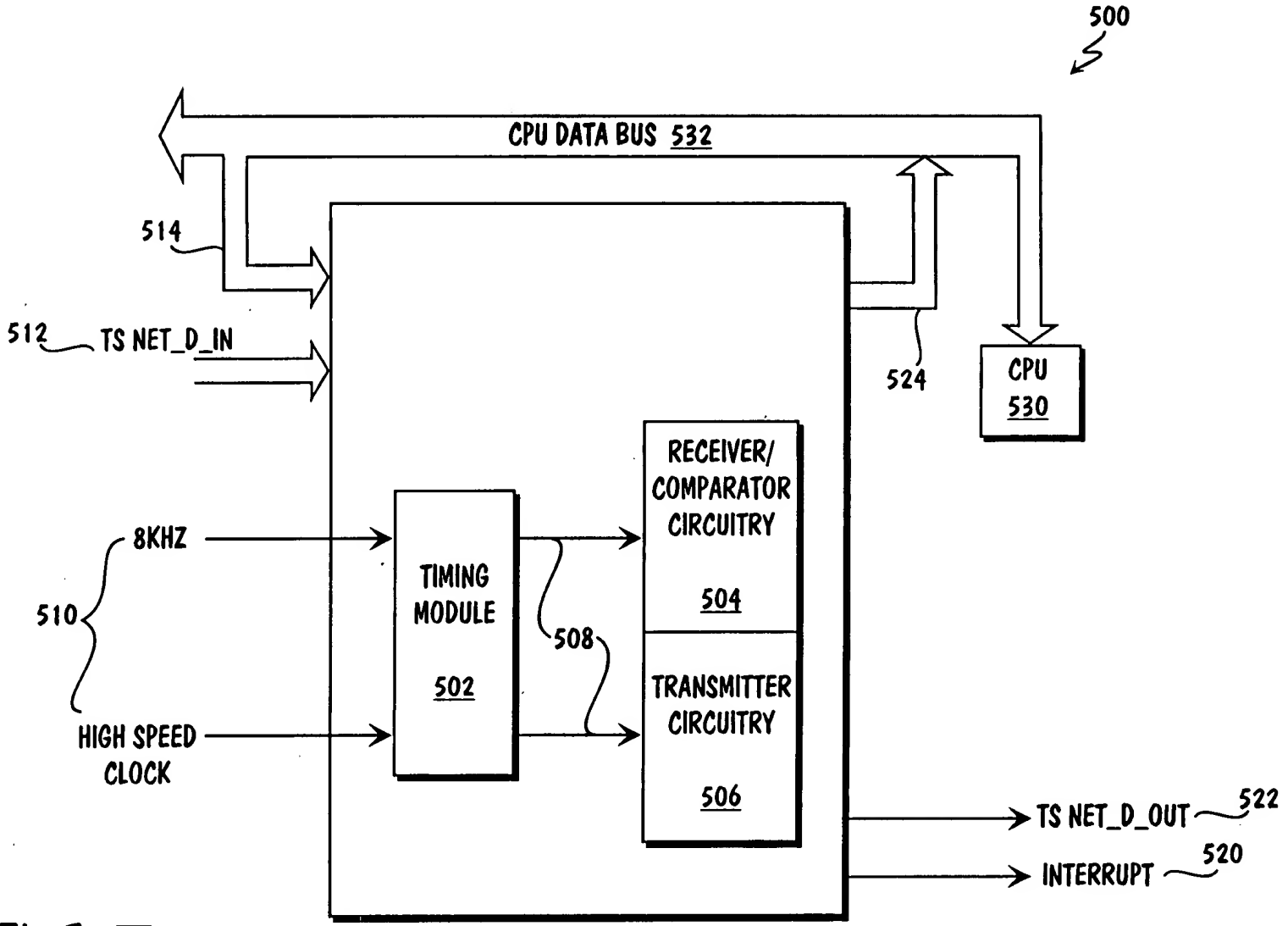

500
CPU DATA BUS 532
514
512
TS NET_D_IN
524
CPU
530
RECEIVER/
COMPARATOR
CIRCUITRY
504
8KHZ
510
TIMING
MODULE
502
508
TRANSMITTER
CIRCUITRY
506
HIGH SPEED
CLOCK
TS NET_D_OUT
522
INTERRUPT
520

FIG. 5

005760 "2T5E9960

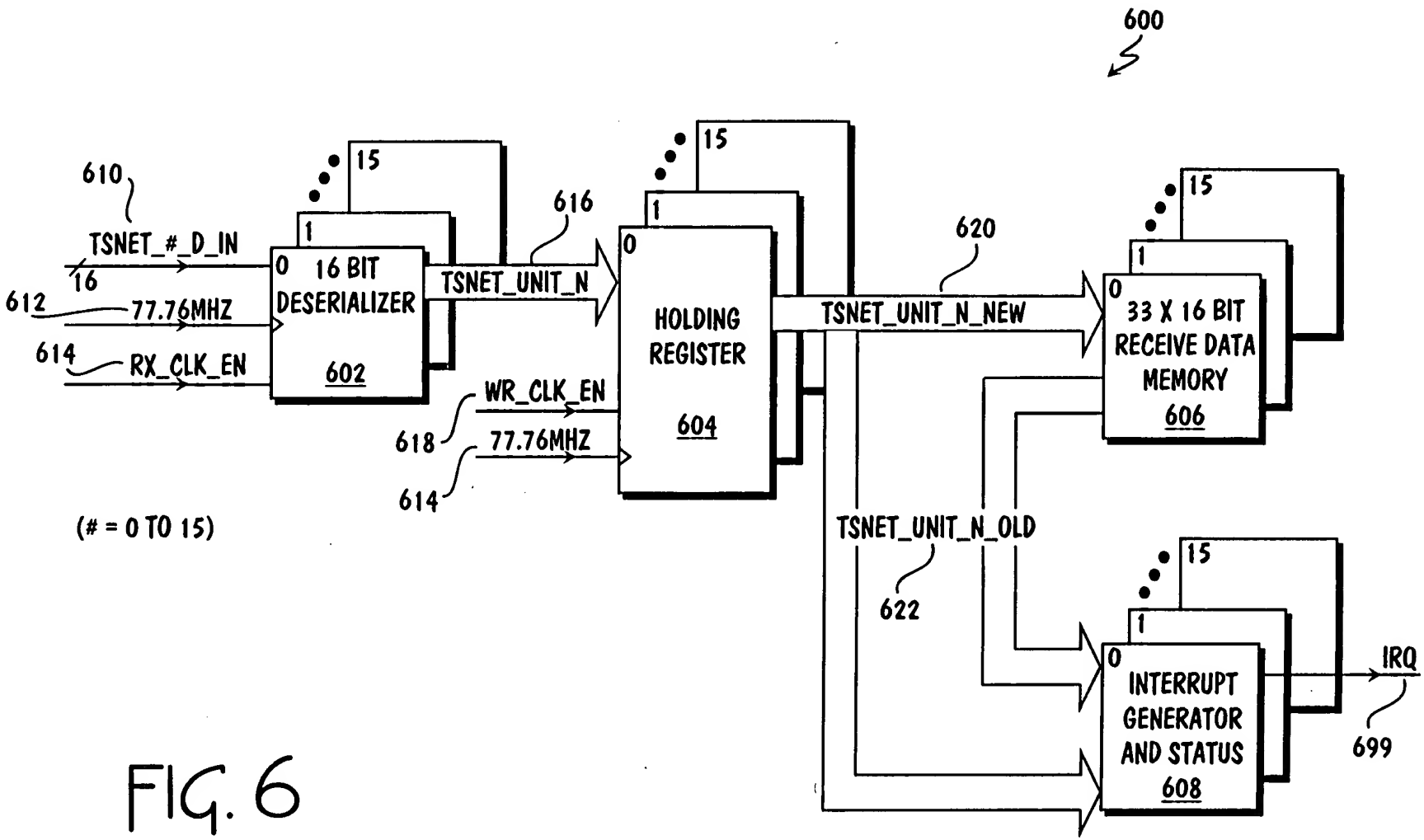


FIG. 6

0057602752969

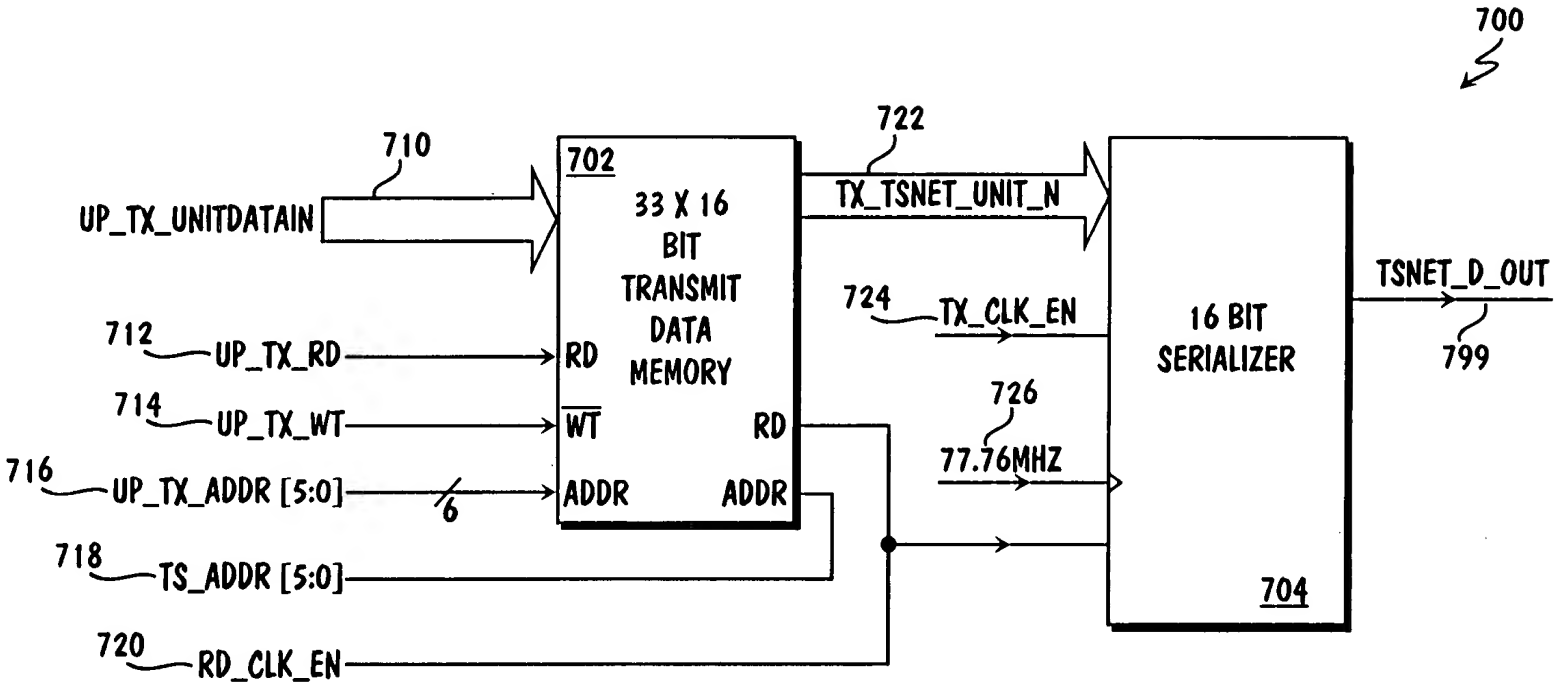


FIG. 7

00560 2756960

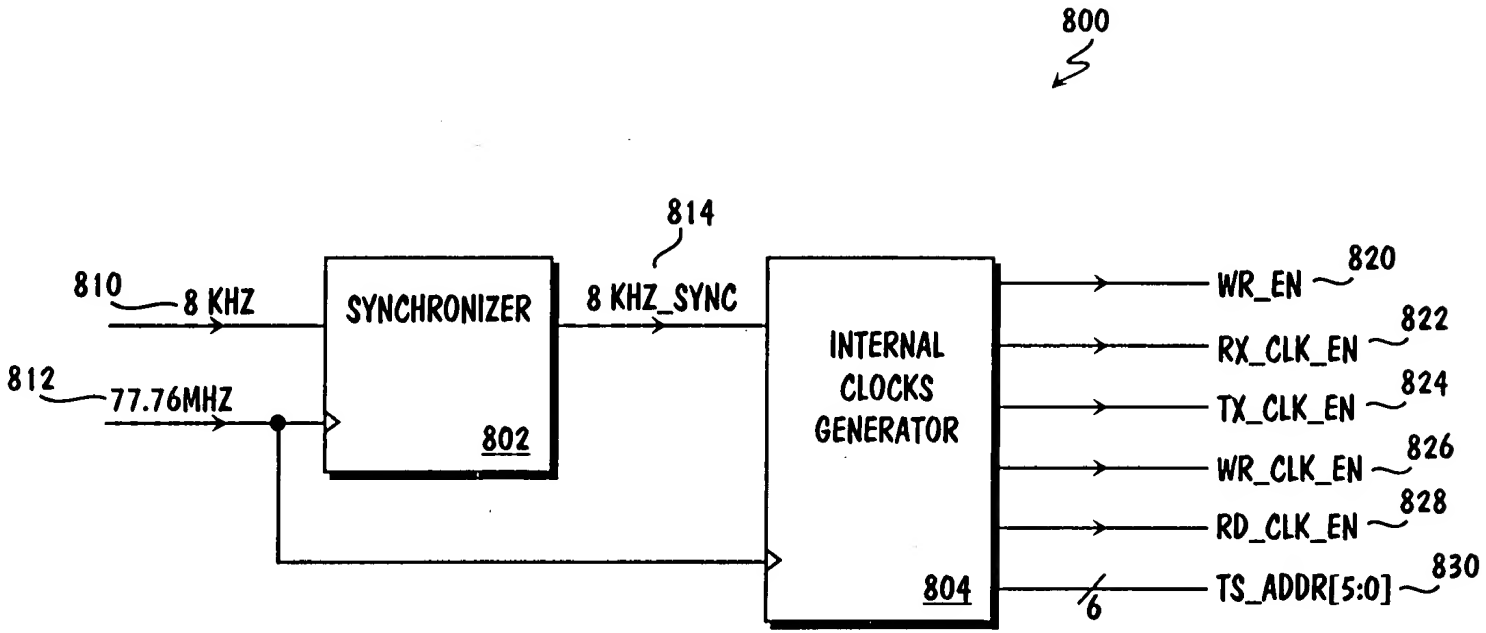


FIG. 8

0057602 2T52960

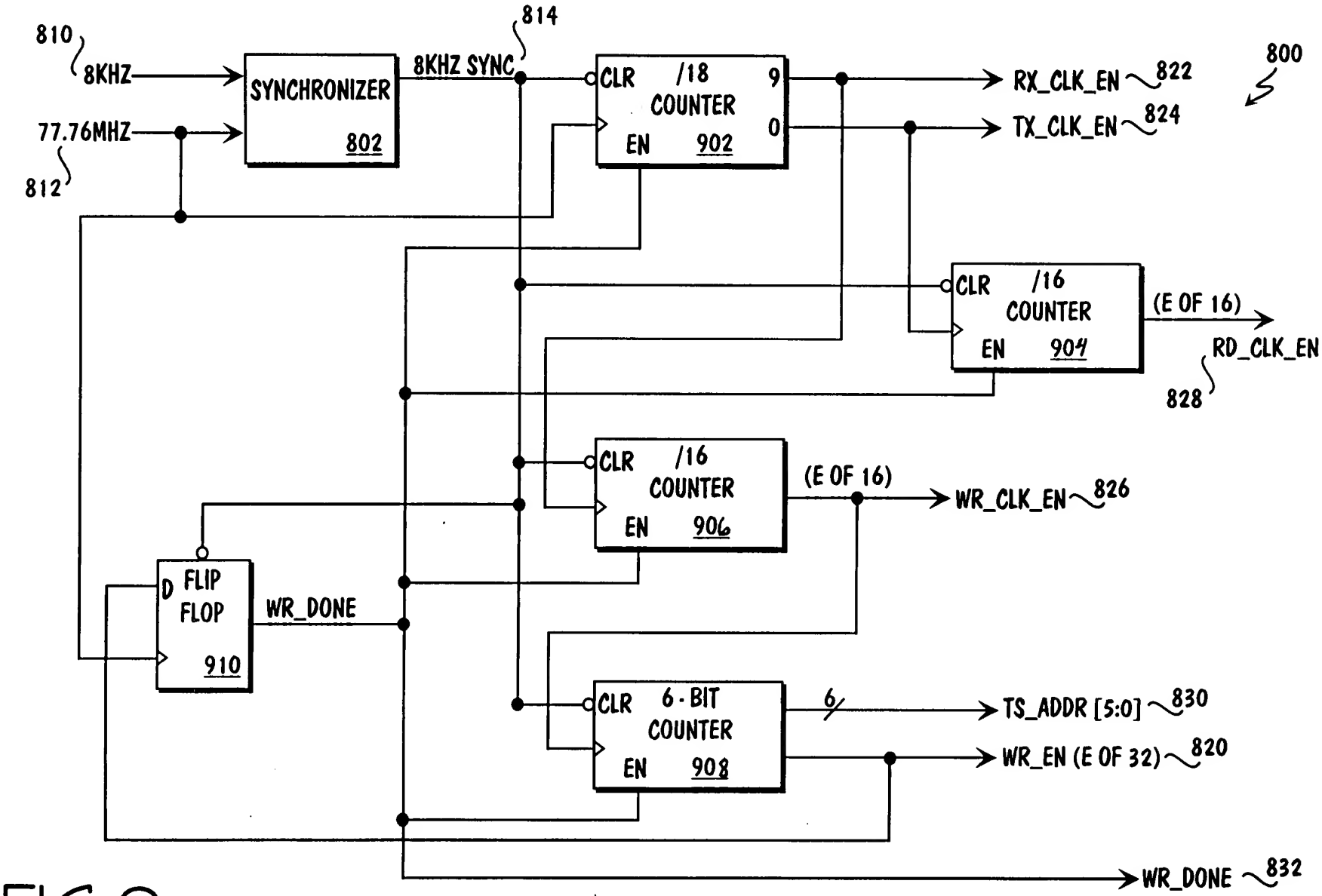


FIG. 9

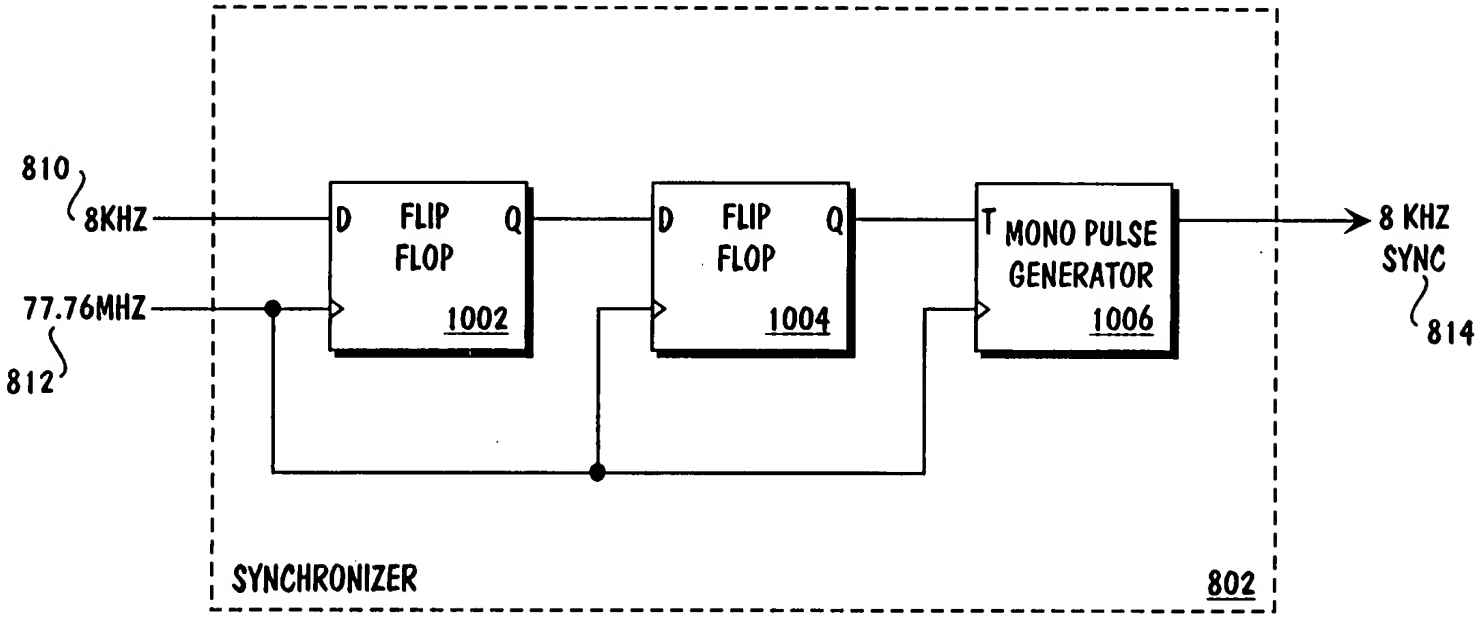

810
8KHZ
77.76MHZ
812
D
FLIP
FLOP
Q
1002
D
FLIP
FLOP
Q
1004
T
MONO PULSE
GENERATOR
1006
8 KHZ
SYNC
814
SYNCHRONIZER
802

FIG. 10

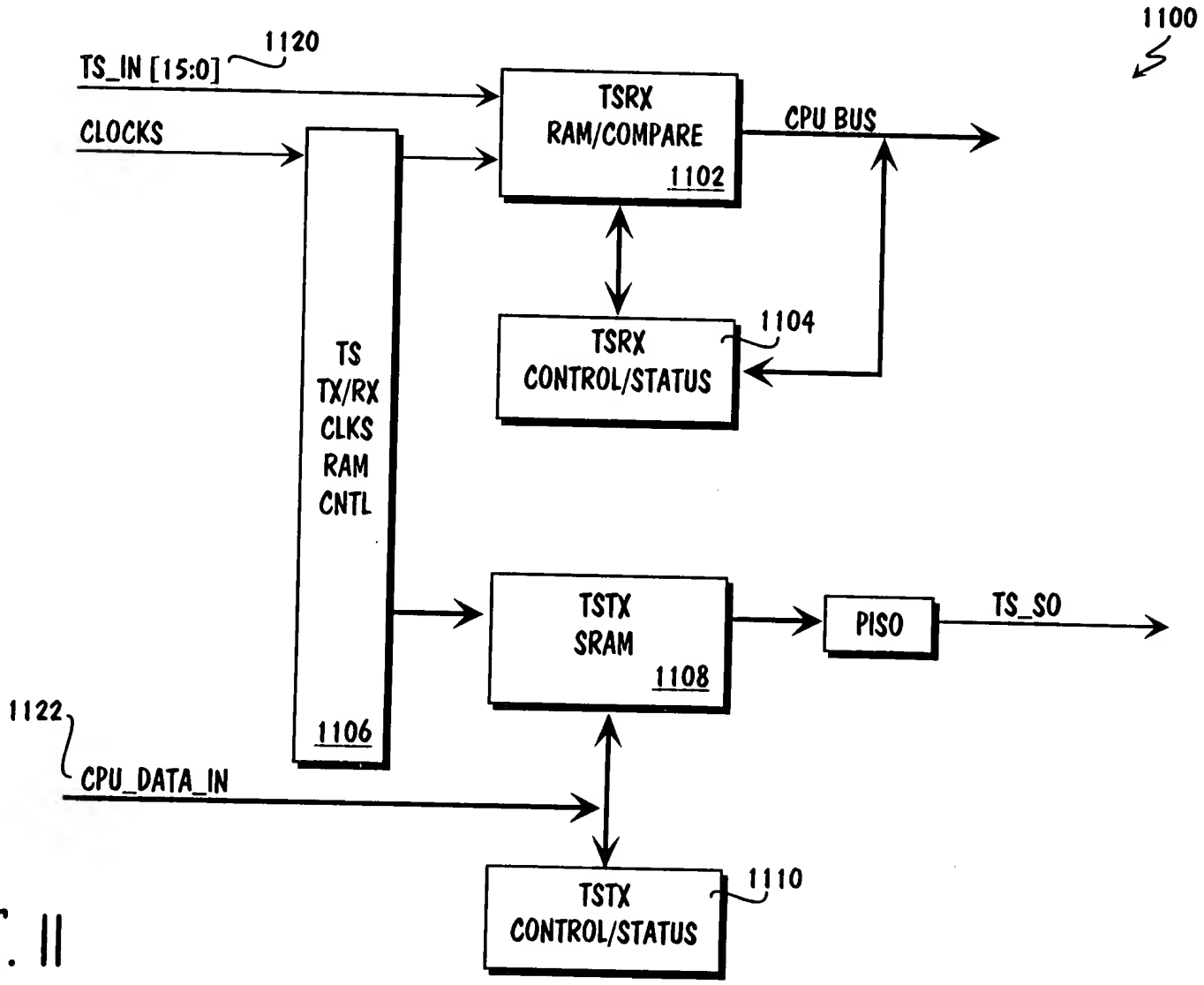

1100
1120
TS_IN [15:0]
CLOCKS
TSRX
RAM/COMPARE
1102
CPU BUS
TSRX
CONTROL/STATUS
1104
TS
TX/RX
CLKS
RAM
CNTL
1106
TSTX
SRAM
1108
PISO
TS_SO
1122
CPU_DATA_IN
TSTX
CONTROL/STATUS
1110

FIG. 11

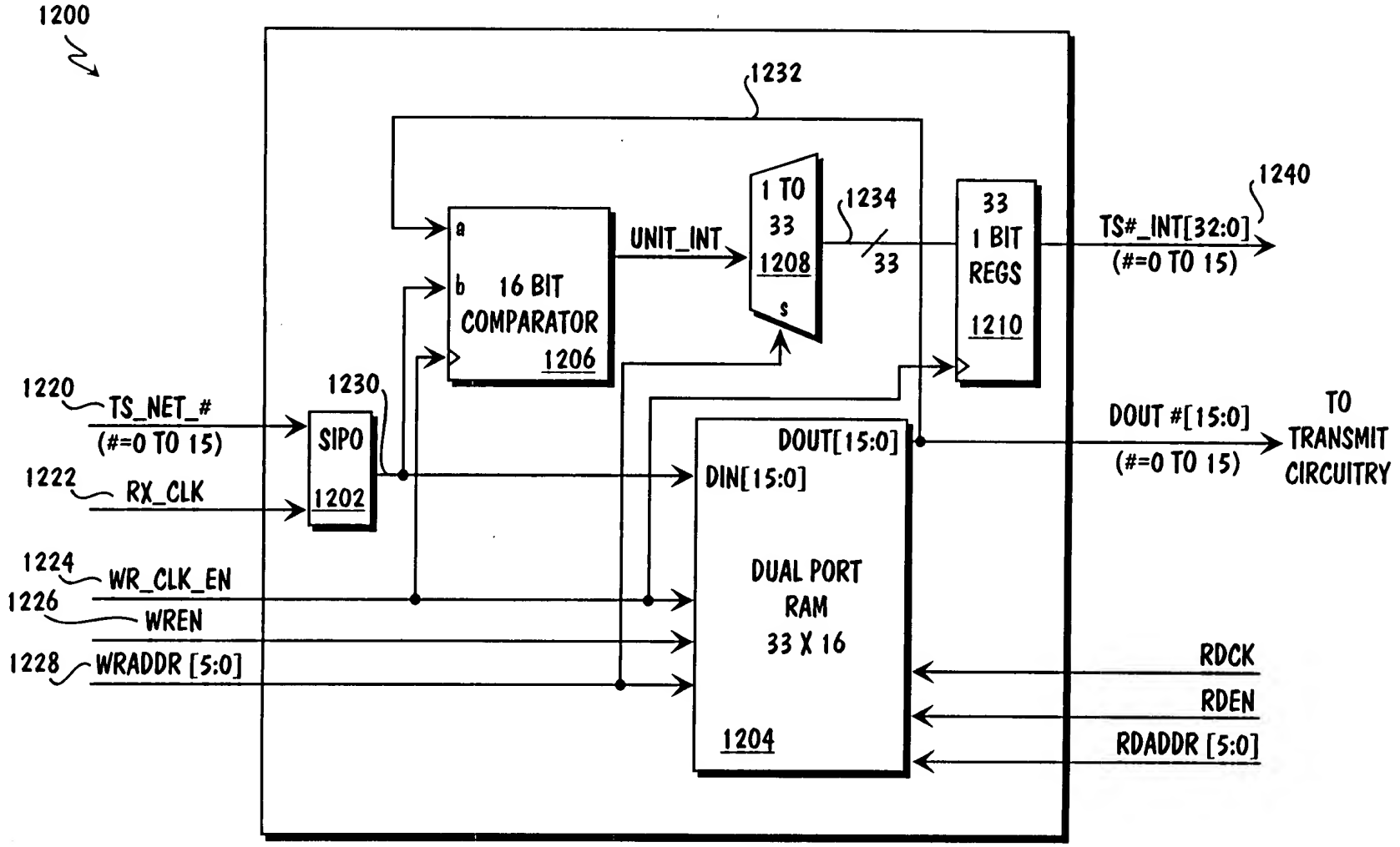

1200
1232
1 TO
33
1208
1234
33
33
1 BIT
REGS
1210
1240
TS#_INT[32:0]
(#=0 TO 15)
a
b
16 BIT
COMPARATOR
1206
UNIT_INT
1230
1220
TS_NET_#
(#=0 TO 15)
SIPO
1202
1222
RX_CLK
1224
WR_CLK_EN
1226
WREN
1228
WRADDR [5:0]
DOUT[15:0]
DIN[15:0]
DUAL PORT
RAM
33 X 16
1204
DOUT #[15:0]
(#=0 TO 15)
TO
TRANSMIT
CIRCUITRY
RDCK
RDEN
RDADDR [5:0]

FIG. 12A

005760 "2T52960

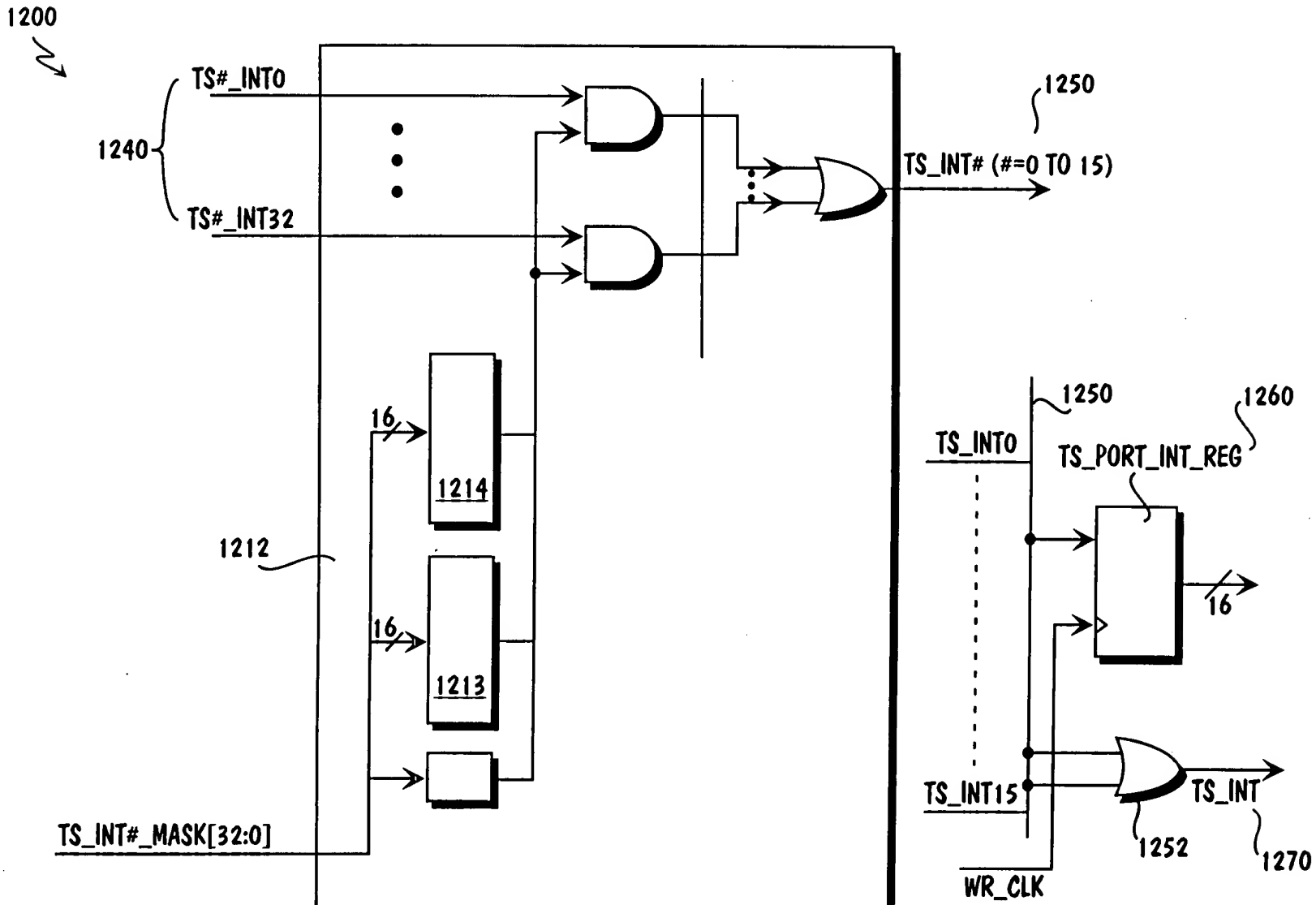


FIG. 12B

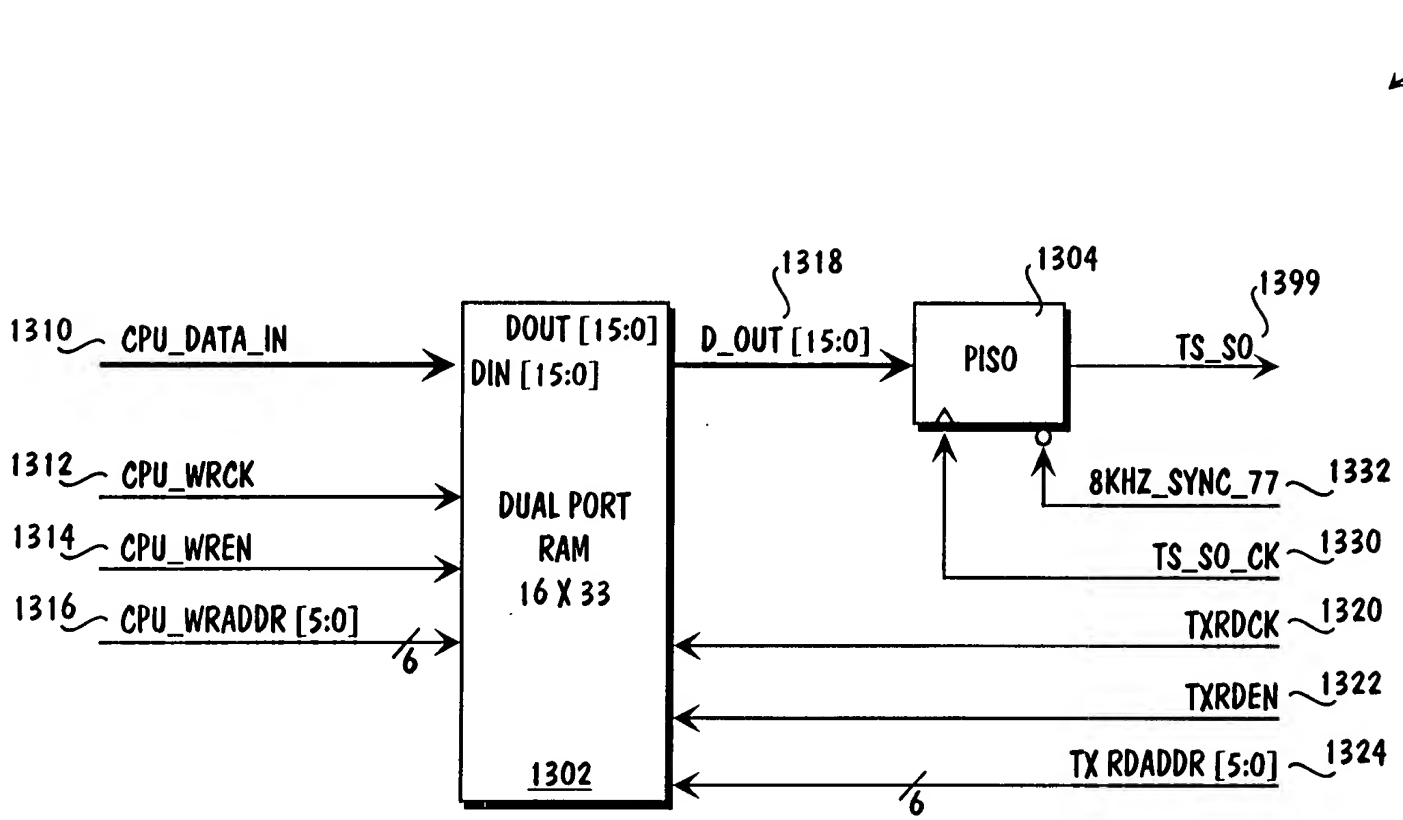

1300
1318
1304
1399
1310
CPU_DATA_IN
DOUT [15:0]
DIN [15:0]
D_OUT [15:0]
PISO
TS_SO
1312
CPU_WRCK
DUAL PORT
RAM
16 X 33
8KHZ_SYNC_77
1332
1314
CPU_WREN
TS_SO_CK
1330
1316
CPU_WRADDR [5:0]
6
TXRDCK
1320
TXRDEN
1322
TX RDADDR [5:0]
1324
6
1302

FIG. 13

Docket No. 2000.019900

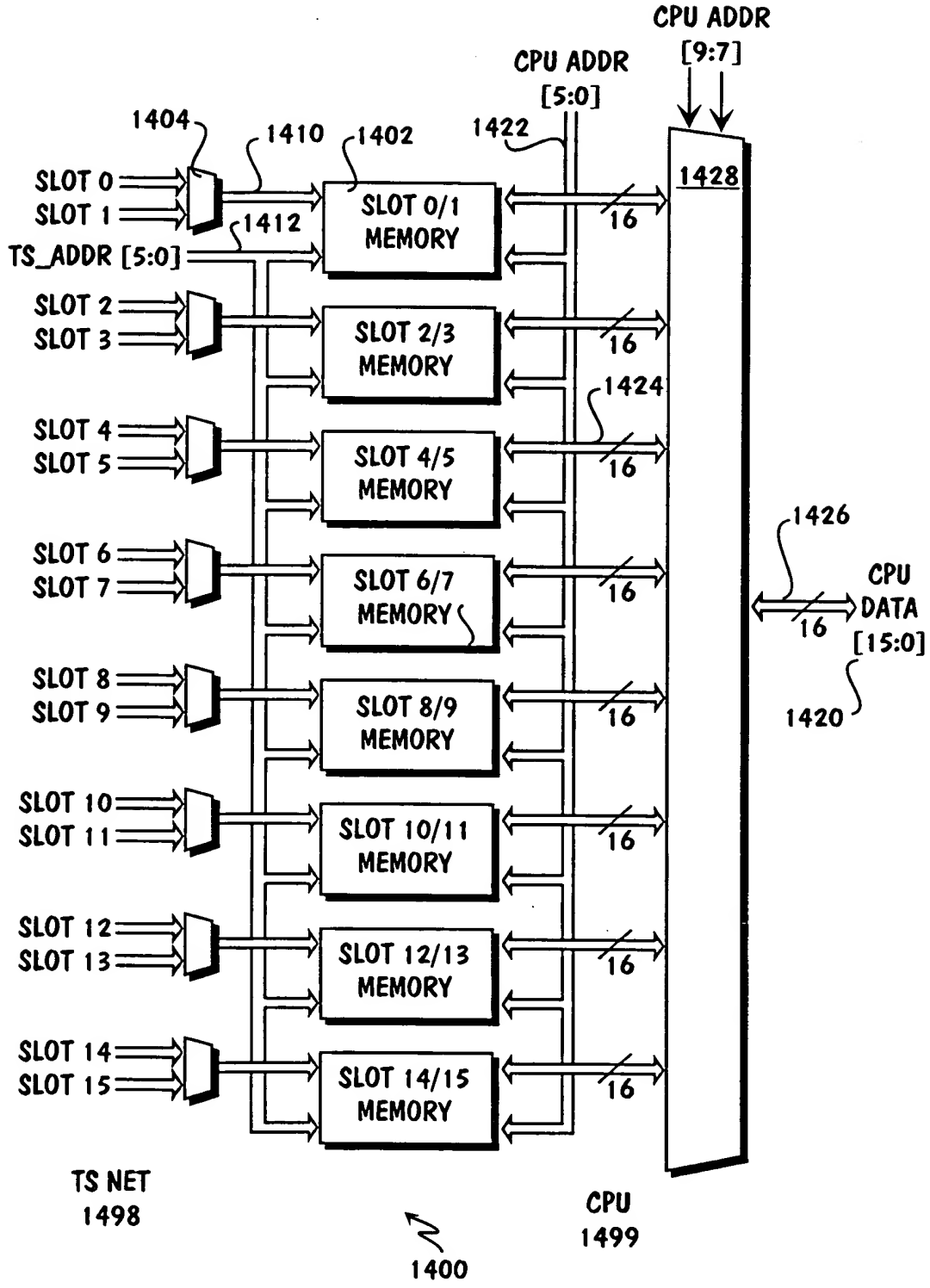


FIG. 14

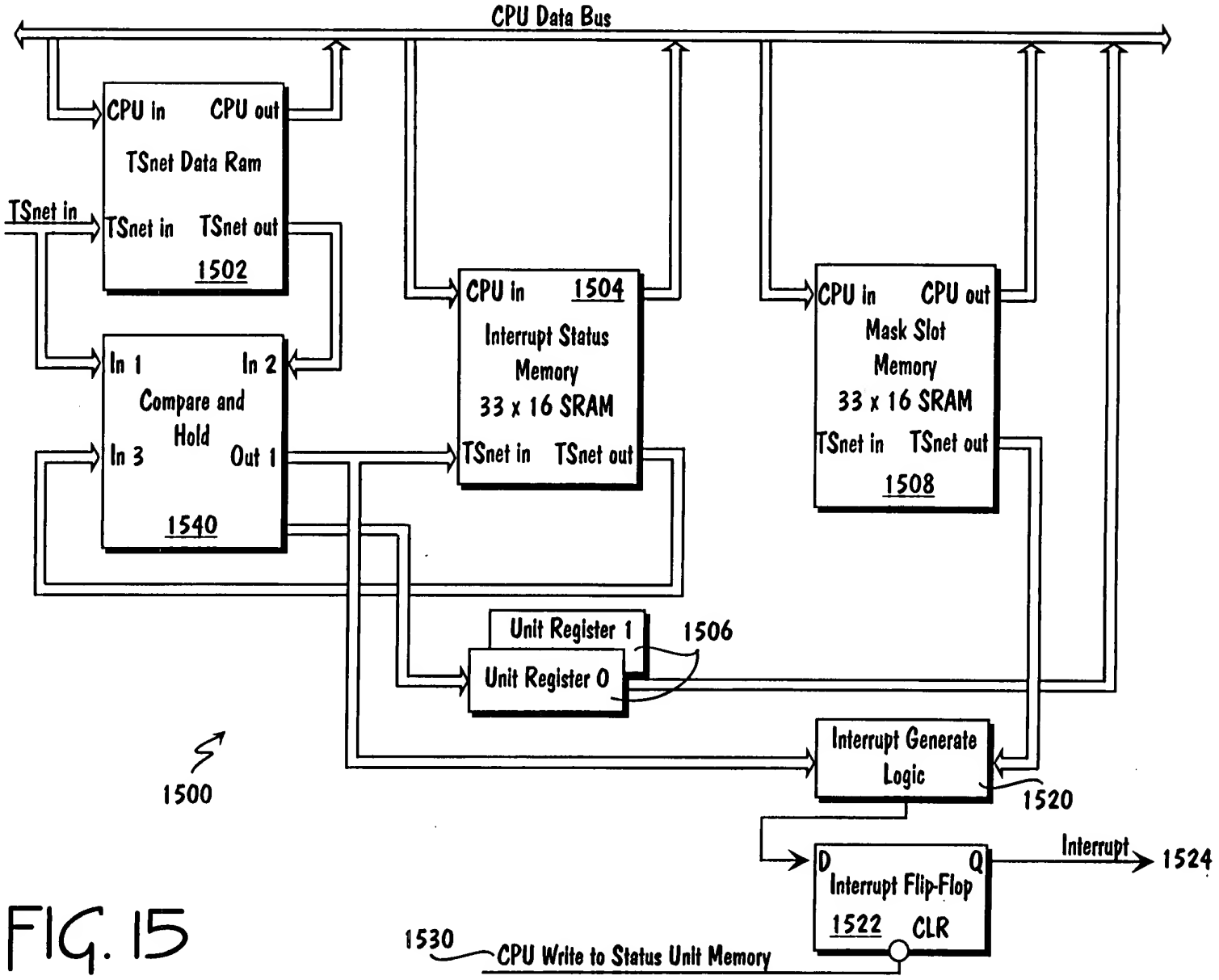
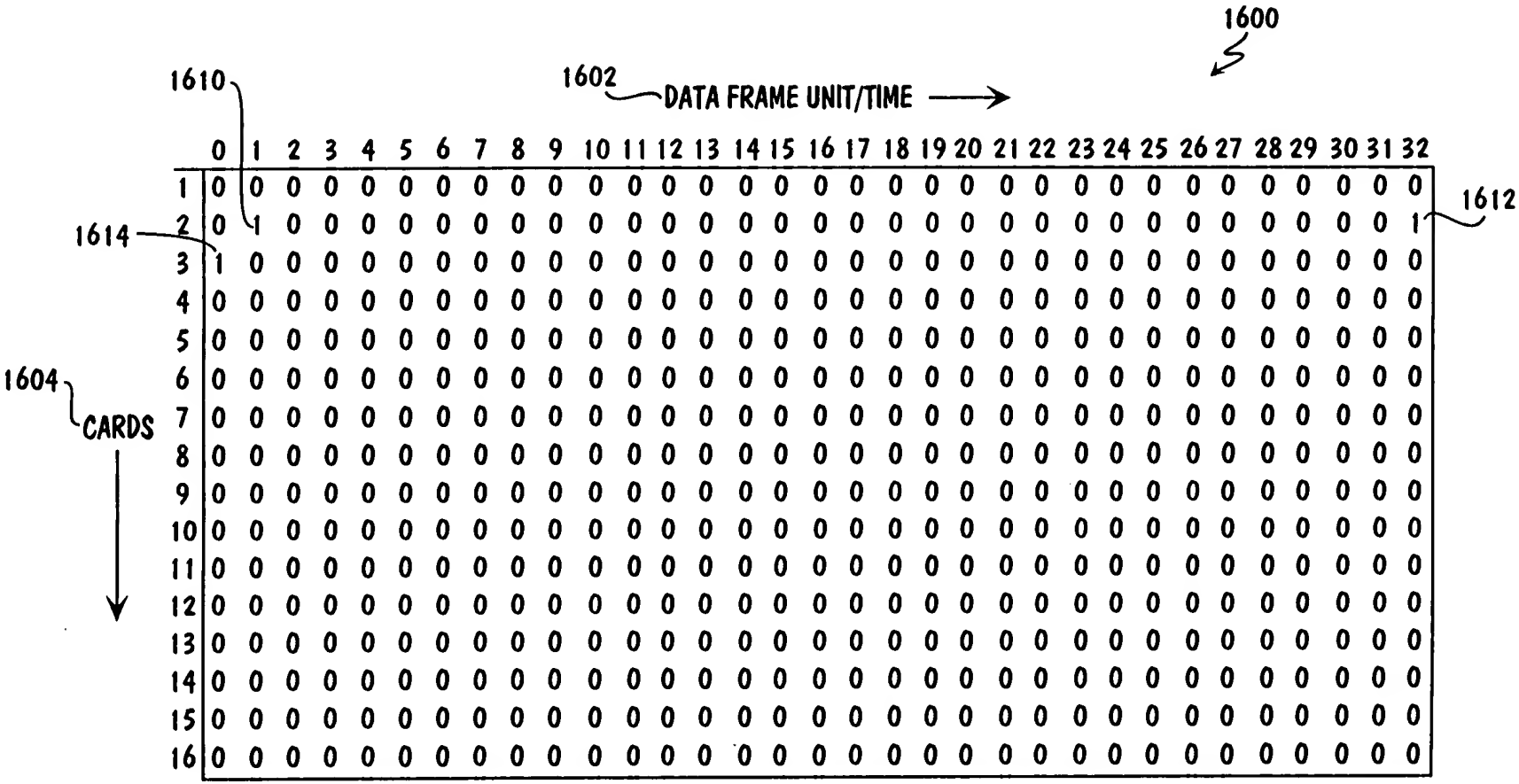

CPU Data Bus
CPU in
CPU out
TSnet Data Ram
TSnet in
TSnet in
TSnet out
1502
CPU in
1504
Interrupt Status
Memory
33 x 16 SRAM
TSnet in
TSnet out
CPU in
CPU out
Mask Slot
Memory
33 x 16 SRAM
TSnet in
TSnet out
1508
In 1
In 2
Compare and
Hold
In 3
Out 1
1540
Unit Register 1
1506
Unit Register 0
1500
Interrupt Generate
Logic
1520
D
Q
Interrupt Flip-Flop
1522
CLR
Interrupt
1524
1530
CPU Write to Status Unit Memory

FIG. 15



	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
3	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIG. 16

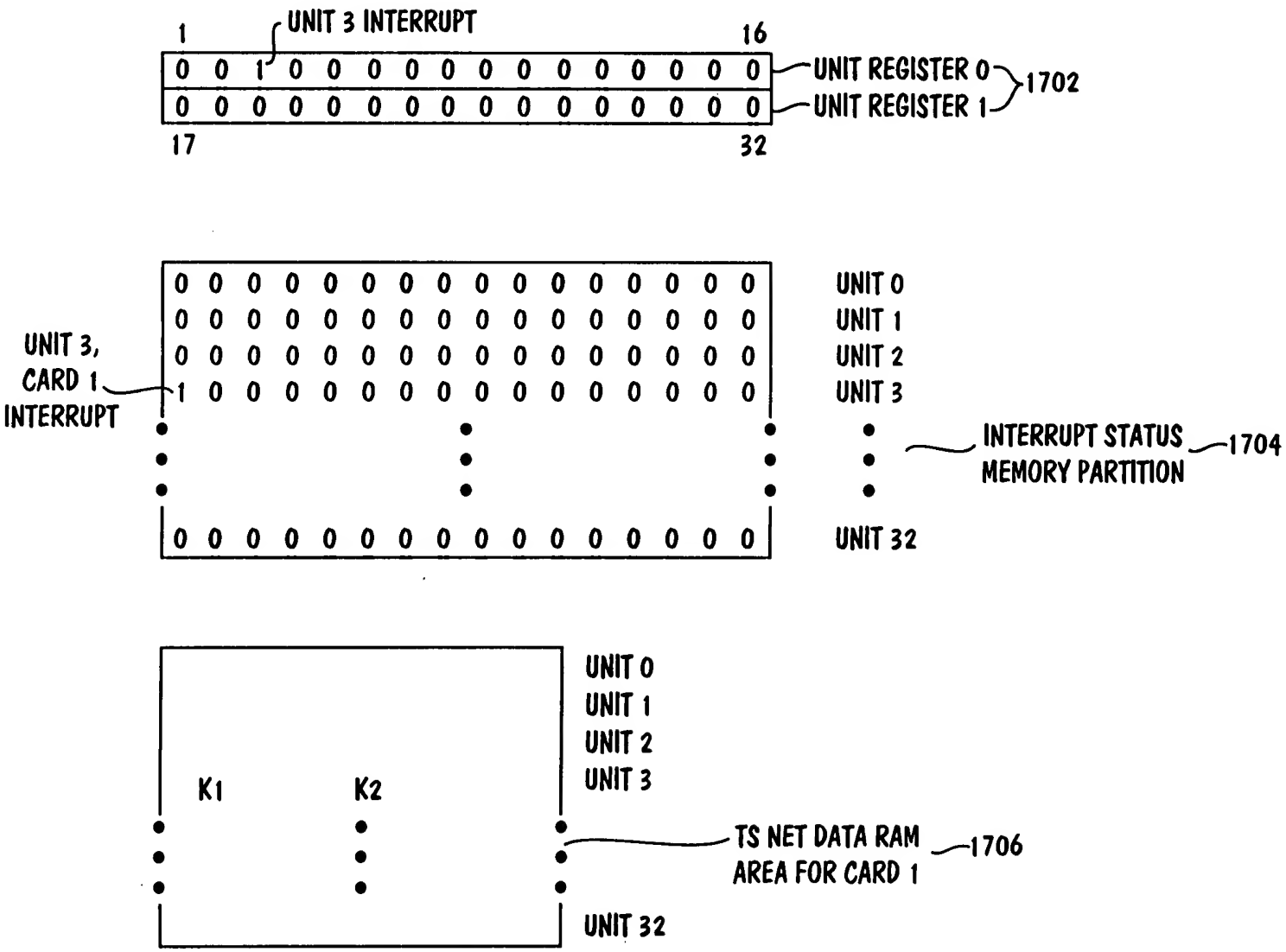

1
UNIT 3 INTERRUPT
16
0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
UNIT REGISTER 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
UNIT REGISTER 1
1702
17
32
UNIT 3,
CARD 1
INTERRUPT
UNIT 0
UNIT 1
UNIT 2
UNIT 3
INTERRUPT STATUS
MEMORY PARTITION
1704
UNIT 32
K1
K2
UNIT 0
UNIT 1
UNIT 2
UNIT 3
TS NET DATA RAM
AREA FOR CARD 1
1706
UNIT 32

FIG. 17

0057602 2TSE9960

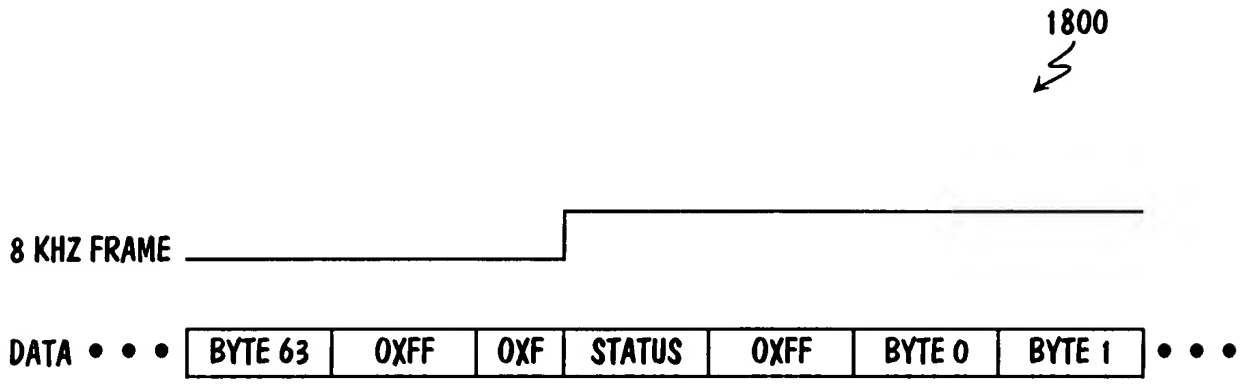


FIG. 18

BIT	7 (MSB)	6	5	4	3	2	1	0 (LSB)
FUNCTION	BRDSTS1	BRDSTS0	1	1	1	1	1	1

STSB1	STSB0	INTERPRETATION
0	0	PRESENT & FAILED (OR NOT BOOTED)
0	1	PRESENT & INACTIVE
1	0	PRESENT & ACTIVE
1	1	NOT PRESENT

FIG. 19

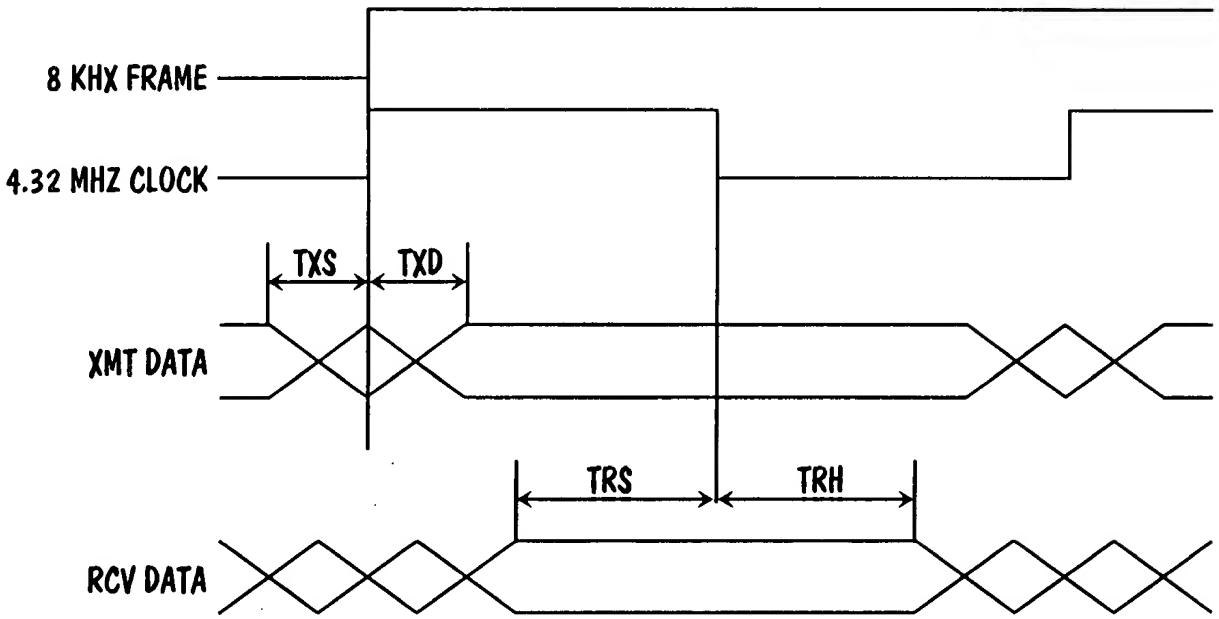


FIG. 20

PARAMETER	DESCRIPTION	MIN	MAX
TXS	TRANSMIT SKEW		30 NSEC
TXD	TRANSMIT DELAY		60 NSEC
TRS	RECEIVE SETUP	30 NSEC	
TRH	RECEIVE HOLD	60 NSEC	

FIG. 21

BYTE		POS.		POS.		POS.	
0	K1 PORT 1	1	K2 PORT 1	2	K1 PORT 2	3	K2 PORT 2
4	K1 PORT 3	5	K2 PORT 3	6	K1 PORT 4	7	K2 PORT 4
8	K1 PORT 5	9	K2 PORT 5	10	K1 PORT 6	11	K2 PORT 6
12	K1 PORT 7	13	K2 PORT 7	14	K1 PORT 8	15	K2 PORT 8
16	K1 PORT 9	17	K2 PORT 9	18	K1 PORT 10	19	K2 PORT 10
20	K1 PORT 11	21	K2 PORT 11	22	K1 PORT 12	23	K2 PORT 12
24	K1 PORT 13	25	K2 PORT 13	26	K1 PORT 14	27	K2 PORT 14
28	K1 PORT 15	29	K2 PORT 15	30	K1 PORT 16	31	K2 PORT 16
32	E1 PORT 1	33	F1 PORT 1	34	SPARE	35	SPARE
36	SPARE	37	SPARE	38	SPARE	39	SPARE
40	SPARE	41	SPARE	42	SPARE	43	SPARE
44	SPARE	45	SPARE	46	SPARE	47	SPARE
48	SPARE	49	SPARE	50	SPARE	51	SPARE
52	SPARE	53	SPARE	54	SPARE	55	SPARE
56	SPARE	57	SPARE	58	SPARE	59	SPARE
60	SPARE	61	SPARE	62	SPARE	63	SPARE

FIG. 22

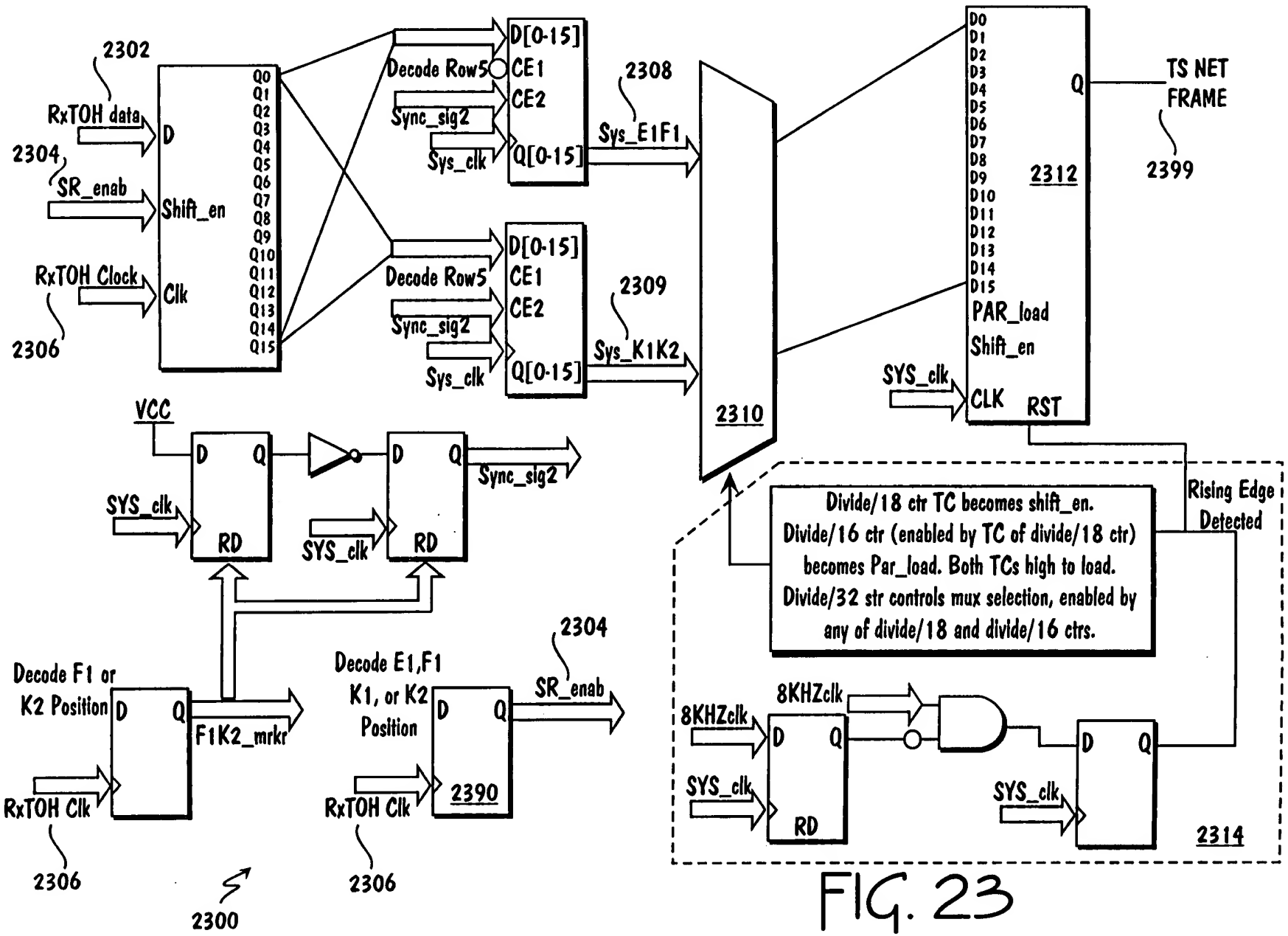

2302
RxTOH data
2304
SR_enab
RxTOH Clock
2306
D
Shift_en
Clk
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Decode Row5
Sync_sig2
Sys_clk
D[0-15]
CE1
CE2
Q[0-15]
2308
Sys_E1F1
2309
Sys_K1K2
2310
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
PAR_load
Shift_en
SYS_clk
CLK
RST
2312
Q
TS NET FRAME
2399
VCC
D
Q
RD
SYS_clk
Sync_sig2
Divide/18 ctr TC becomes shift_en.
Divide/16 ctr (enabled by TC of divide/18 ctr) becomes Par_load. Both TCs high to load.
Divide/32 str controls mux selection, enabled by any of divide/18 and divide/16 ctrs.
Rising Edge Detected
Decode F1 or K2 Position
F1K2_mrkr
Decode E1,F1 K1, or K2 Position
2390
2304
SR_enab
RxTOH Clk
2306
2300
8KHZclk
2314

FIG. 23

0057602 2759960

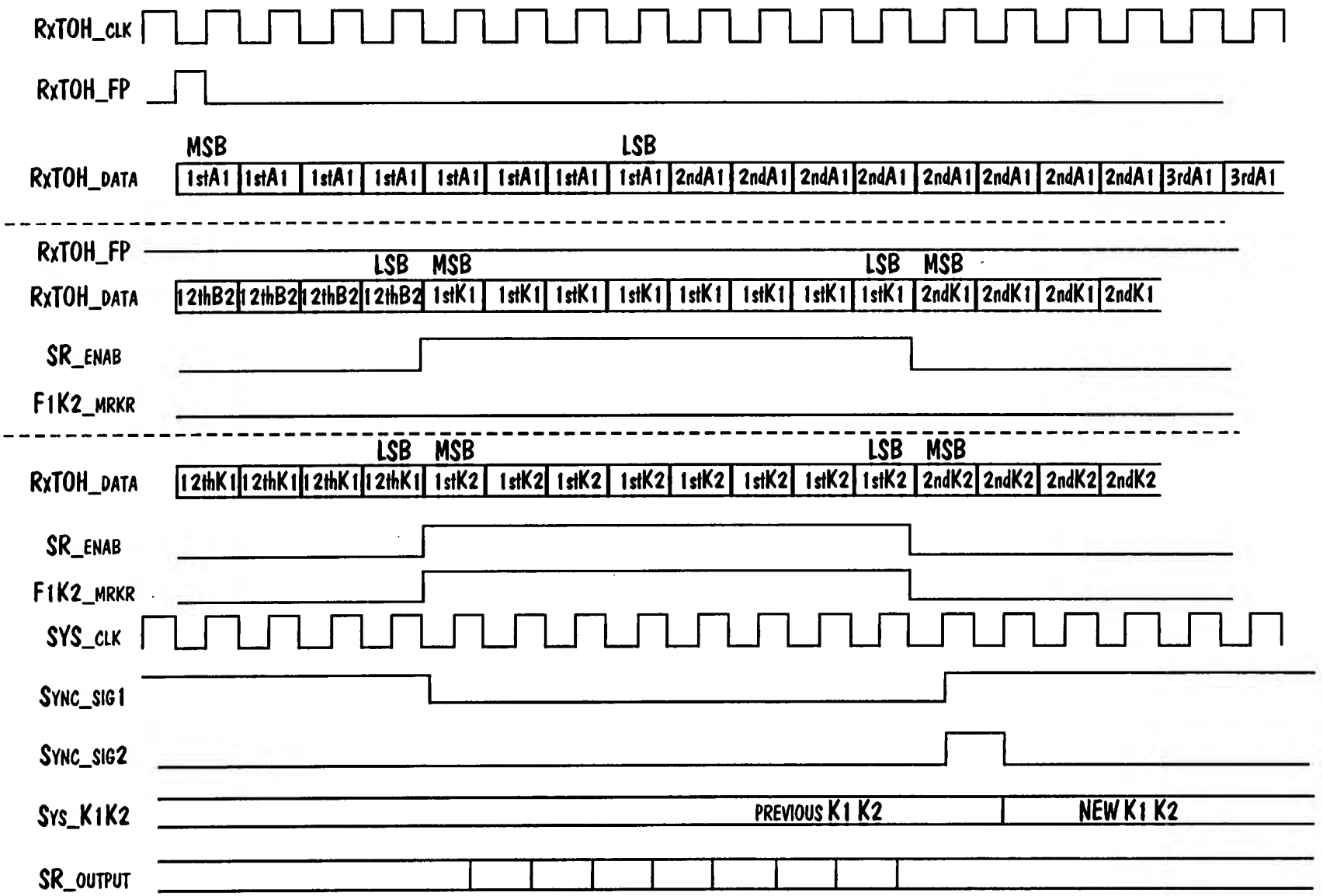


FIG. 24

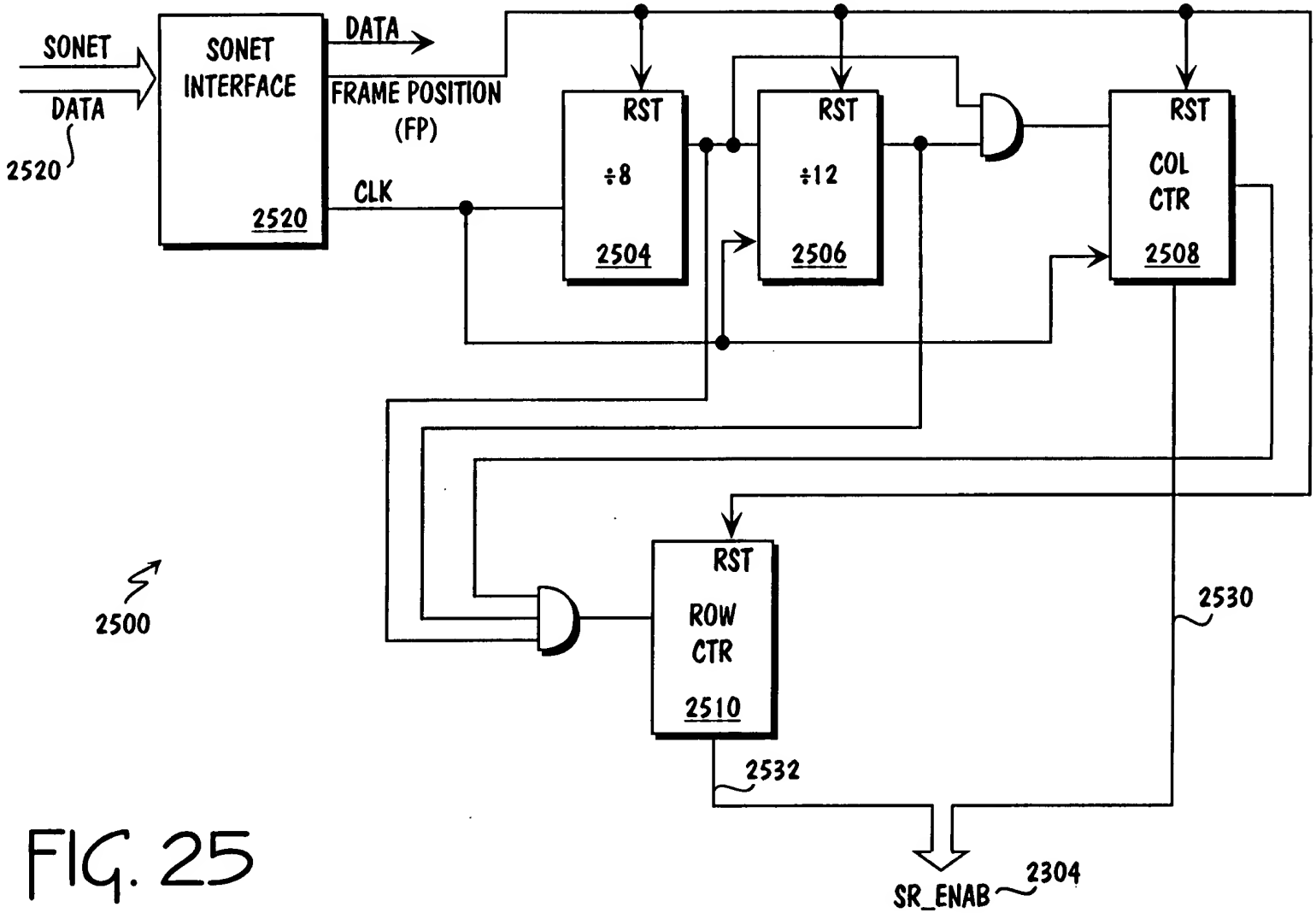

SONET
DATA
2520
SONET INTERFACE
2520
DATA
FRAME POSITION (FP)
CLK
RST
÷8
2504
RST
÷12
2506
RST
COL CTR
2508
RST
ROW CTR
2510
2500
2530
2532
SR_ENAB
2304

FIG. 25

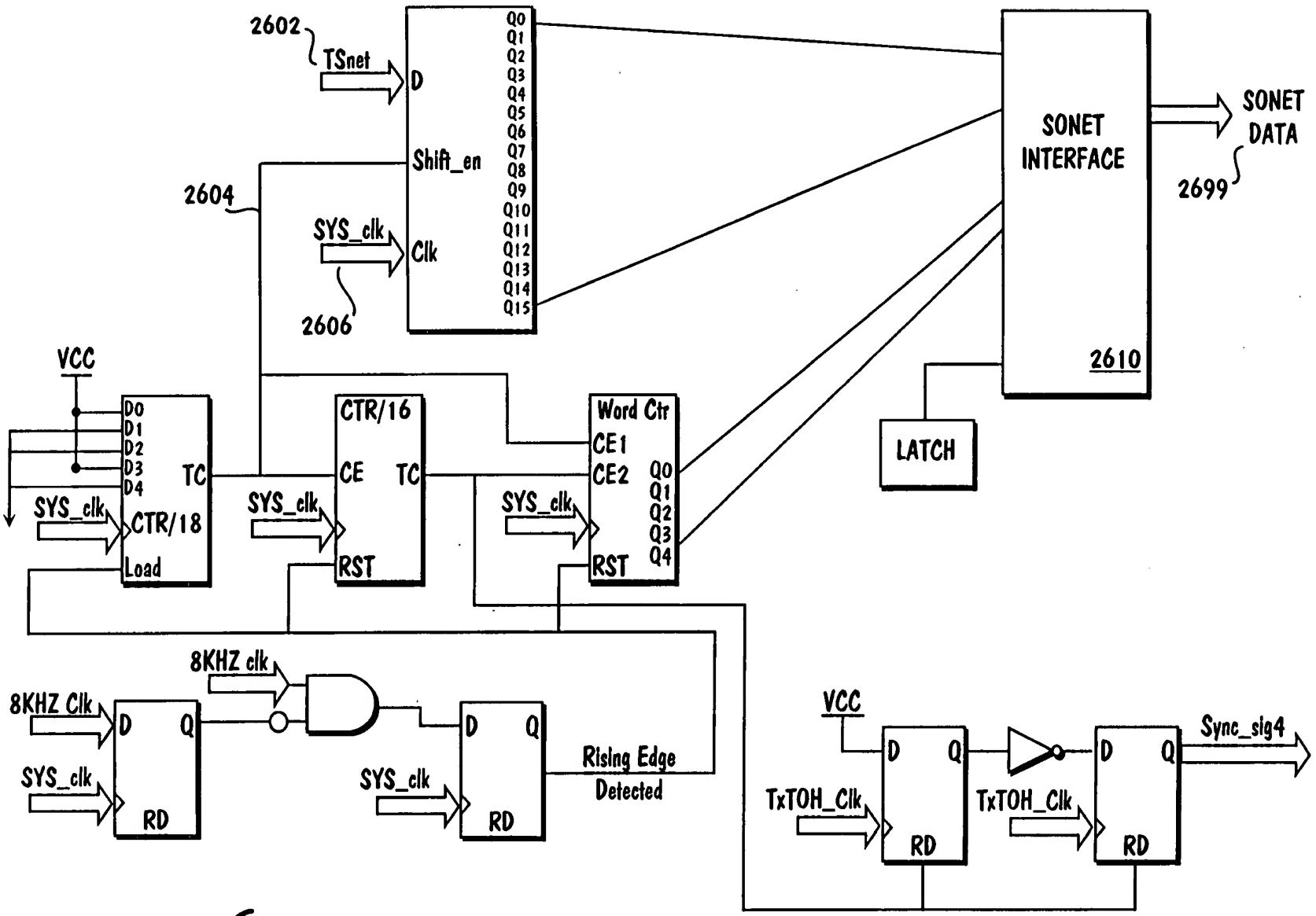

2602
TSnet
D
Shift_en
2604
SYS_clk
Clk
2606
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
SONET INTERFACE
2610
SONET DATA
2699
LATCH
VCC
D0
D1
D2
D3
D4
TC
SYS_clk
CTR/18
Load
CTR/16
CE
TC
SYS_clk
RST
Word Ctr
CE1
CE2
Q0
Q1
Q2
Q3
Q4
SYS_clk
RST
8KHZ clk
8KHZ Clk
D
Q
SYS_clk
RD
D
Q
SYS_clk
RD
Rising Edge Detected
VCC
D
Q
TxTOH_Clk
RD
TxTOH_Clk
D
Q
RD
Sync_sig4

FIG. 26

0956754 0956750

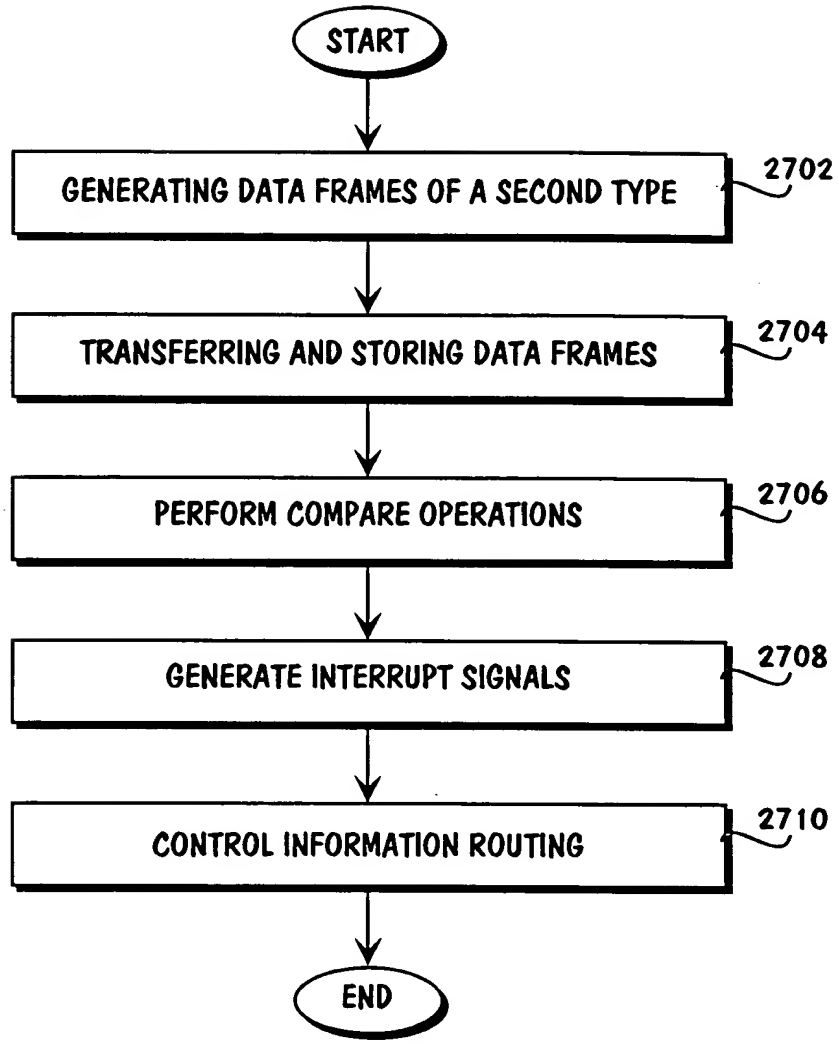


FIG. 27

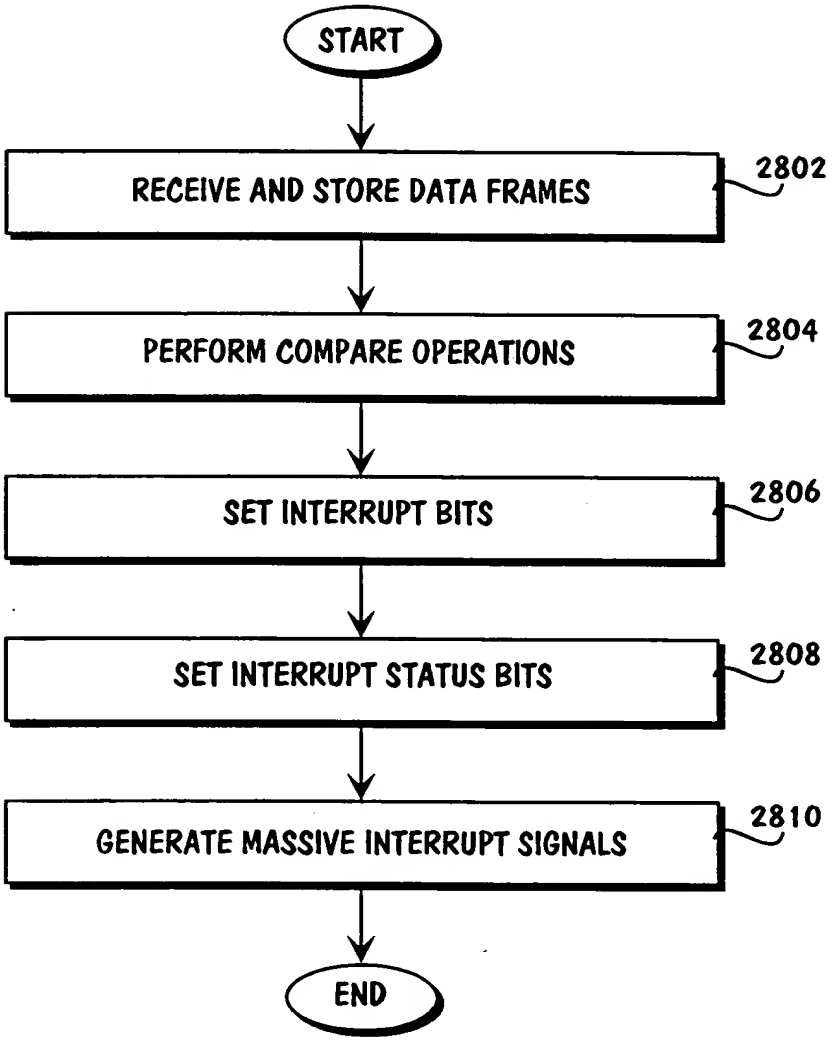

START
RECEIVE AND STORE DATA FRAMES
2802
PERFORM COMPARE OPERATIONS
2804
SET INTERRUPT BITS
2806
SET INTERRUPT STATUS BITS
2808
GENERATE MASSIVE INTERRUPT SIGNALS
2810
END

FIG. 28

0057650 - 2156960

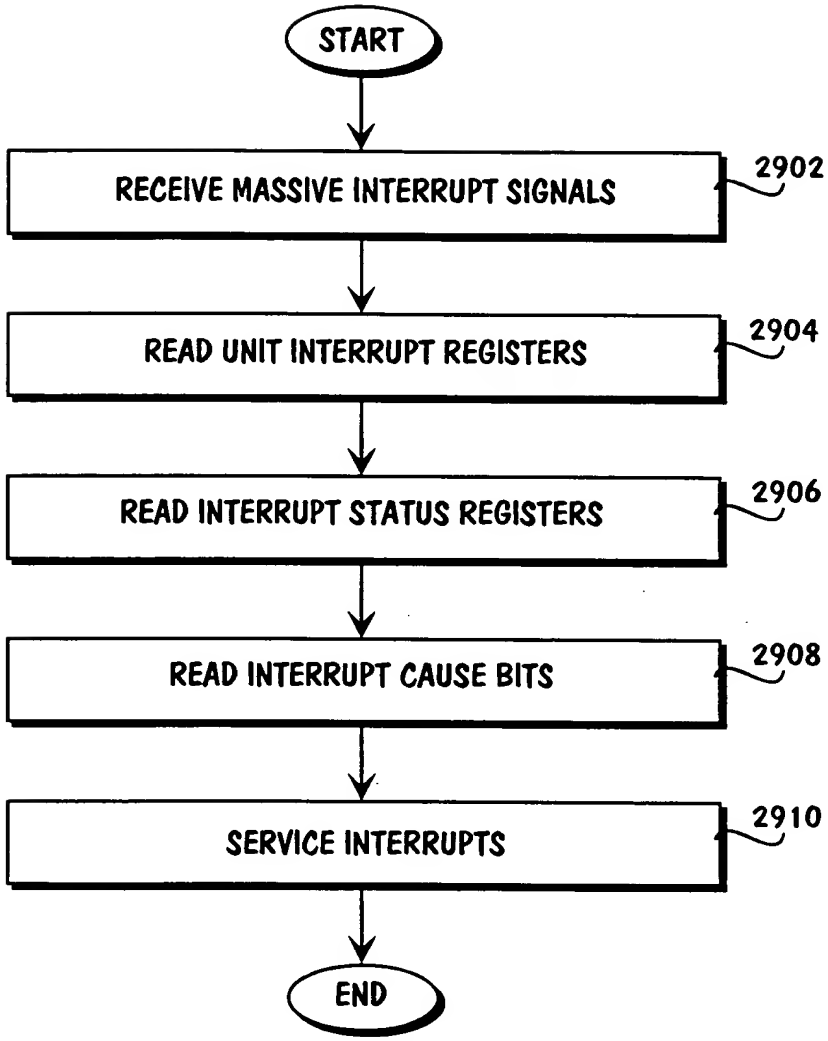


FIG. 29